[Attorney list on signature page]

IN THE UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA – SAN JOSE DIVISION

RAMBUS INC., Plaintiff, v. HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A., Defendants.	Case No. C 05-00334 RMW **MANUFACTURERS' JOINT MOTION FOR SUMMARY JUDGMENT OF (1) NON-INFRINGEMENT OF THE FARMWALD PATENTS UNDER THE MANUFACTURERS' PROPOSED CLAIM CONSTRUCTION, OR (2) INVALIDITY OF THE FARMWALD PATENTS UNDER RAMBUS'S PROPOSED CLAIM CONSTRUCTION AND MEMORANDUM OF POINTS AND AUTHORITIES** Date: March 26, 2008 Time: 9:00 a.m. Hon. Ronald M. Whyte
RAMBUS INC., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., Defendants.	Case No. C 05-02298 RMW
RAMBUS INC., Plaintiff, v. MICRON TECHNOLOGY, INC. and MICRON SEMICONDUCTOR PRODUCTS, INC., Defendants.	Case No. C 06-00244 RMW

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NOTICE OF MOTION AND MOTION

TO ALL PARTIES AND THEIR ATTORNEYS OF RECORD:

PLEASE TAKE NOTICE that on March 26, 2008, at 9:00 a.m. or as soon thereafter as this matter may be heard, Defendants Samsung Electronics Co., Ltd,. Samsung Electronics America, Inc., and Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P., ("Samsung"); Hynix Semiconductor Inc., Hynix Semiconductor America Inc., and Hynix Semiconductor Manufacturing America, Inc., ("Hynix"); Nanya Technology Corporation and Nanya Technology Corporation U.S.A. ("Nanya"); and Micron Technology, Inc. and Micron Semiconductor Products, Inc. ("Micron") (collectively "the Manufacturers"), [1] will and hereby do move this Court for an order granting summary judgment of noninfringement under the Manufacturers' proposed claim constructions or summary judgment of invalidity under Rambus's proposed claim constructions. The Manufacturers jointly file this Notice of Motion, Motion for Summary Judgment, and Memorandum of Points and Authorities pursuant to the Joint Case Management Order dated April 24, 2007.

RELIEF REQUESTED

Pursuant to Rule 56 of the Federal Rules of Civil Procedure, the Manufacturers respectfully seek an Order granting summary judgment of noninfringement in favor of the Manufacturers on Samsung's 2nd Affirmative Defense and Count VIII in its counterclaims; Hynix's 2nd Affirmative Defense and counterclaim 6; Nanya's 2nd Affirmative Defense and counterclaim 5; and Micron's 2nd Affirmative Defense and Counts I-XIV in its counterclaims. Alternatively, if the Court adopts any of Rambus's proposed claim constructions, the Manufacturers seek an Order granting summary judgment of invalidity in favor of the Manufacturers on Samsung's 3rd Affirmative Defense and Count IX in its counterclaims; Hynix's 3rd Affirmative Defense and counterclaim 7; Nanya's 3rd Affirmative Defense and counterclaim 6; and Micron's 4th Affirmative Defense and Counts I-XIV in its counterclaims.

[1] As indicated in the Joint Claim Construction Statement ("JCCS"), not all "asserted claims" have been asserted (or timely asserted) against all Manufacturers. Each Manufacturer's arguments herein pertain only to those claims that have been timely asserted against that Manufacturer.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

If the Court adopts the Manufacturers' argument that the proper construction of the disputed claim terms in the Farmwald patents-in-suit are the ones that most naturally align with the patents' description of the purported invention, then none of the asserted claims are infringed. Alternatively, if the Court adopts the broad claim constructions proposed by Rambus, then each of the asserted claims fails to meet the written description requirement of 35 U.S.C § 112, ¶ 1 and/or the subject matter requirement of § 112, ¶ 2, and is therefore invalid.

When Rambus drafted the common specification of the Farmwald patents-in-suit, it distinguished its purported invention from pre-existing, conventional memory designs employed by the Manufacturers and others in the industry based on three requirements: (1) a memory device that interfaces to a narrow multiplexed bus; (2) read and write requests transmitted in the form of request packets; and (3) a clocking scheme that uses an early clock and a late clock to derive timing information. These requirements are discussed throughout the Farmwald patents-in-suit, and described as "the present invention." Rambus's purported invention stands in stark contrast to the Accused Products (as defined herein), which use the conventional design rejected by Rambus.

As the datasheets for each of the Manufacturers' representative products show, the Accused Products do not satisfy any of these requirements. Rather, they use the traditional wide-bus design in which commands are sent along separate dedicated signal lines in synchronization with a single clock. There is no genuine dispute about the structure and function of the Accused Products, as described in the datasheets (which were cited by Rambus in its preliminary infringement contentions). Summary judgment of noninfringement is therefore appropriate if the Court adopts the Manufacturers' proposed constructions for the term "device," the transaction terms set forth in Appendix B to the Manufacturers' claim construction brief, or the clocking terms set forth in Appendix C to the Manufacturers' claim construction brief.

In an effort to preserve its infringement positions, Rambus has proposed broad constructions divorced from the disclosures in the specification. If adopted, these constructions

would render each of the asserted claims invalid under 35 U.S.C § 112 as unsupported by the specification.

In short, summary judgment in favor of the Manufacturers is appropriate under either party's proposed claim constructions. Under the Manufacturers' proposed constructions, the Accused Products do not infringe the asserted claims as a matter of law. Under Rambus's proposed constructions, the asserted claims are invalid for lack of an adequate written description.

II. OVERVIEW OF THE FARMWALD PATENTS-IN-SUIT

The Farmwald patents-in-suit are directed to a single, narrow, high-speed multiplexed bus for communication between a processor and other devices, including memory devices adapted for use in this bus system. As the common specification[2] explains, this single multiplexed bus carries address, data and control information without the need for a separate device-select line. The common specification also explains that all transaction requests (*e.g.*, read and write requests) to be sent to the memory devices in the form of request packets. The Farmwald patents-in-suit also require a specific "early clock/late clock" system is required to implement this narrow multiplexed bus.

Rambus has alleged infringement of the following claims by all of the Manufacturers: U.S. Patent No. 6,182,184 claim 14; U.S. Patent No. 6,266,285 claims 1 and 16; U.S. Patent No. 6,314,051 claims 27, 32 and 43; 6,493,789 claim 13; U.S. Patent No. 6,496,897 claim 2, 16; U.S. Patent No. 6,546,446 claims 2, 3 and 4; U.S. Patent No. 6,584,037 claims 1, 9 and 34; U.S. Patent No. 6,697,295 claim 45; U.S. Patent No. 6,715,020 claims l, 2 and 14; and U.S. Patent No. 6,751,696 claim 4. In addition, Rambus has accused Nanya and Samsung of infringing U.S. Patent No. 6,324,120 claim 33; U.S. Patent No. 6,378,020 claim 36; U.S. Patent No. 6,426,916 claim 28; and U.S. Patent No. 6,452,863 claim 16. Samsung is also accused of infringing U.S. Patent No. 6,038,195 claim 1.[3]

[2] "The common specification" or "the specification" refers to the parent '898 Application, filed April 18, 1990. The Farmwald patents-in-suit all issued from applications that are continuations of the '898 Application and thus include the same disclosure.

[3] This motion does not address any additional contentions first raised by Rambus in its Counter-claims in Reply filed on July 9, 2007 which are the subject of pending motions.

III. OVERVIEW OF THE ACCUSED PRODUCTS

In accordance with the Court's instructions at the May 24, 2007 hearing, the Manufacturers have identified representative parts for each product accused of infringement by Rambus ("the Accused Products").[4,5,6,7] Exemplary data sheets for some of these representative parts are cited herein and in the accompanying Declaration of Joseph McAlexander In Support Of The Manufacturers' Farmwald and Ware Motions For Summary Judgment ("McAlexander SJ Decl."). There are no relevant differences between the Manufacturers' representative products with respect to the specific features and functionality addressed in this motion.[8] *See generally* McAlexander SJ Decl.

IV. SUMMARY JUDGMENT OF NONINFRINGEMENT

As demonstrated herein and in the accompanying declaration of Joseph McAlexander, adoption of the Manufacturers' proposed claim constructions for the "device" terms set forth in

[4] Samsung Part No. K4D261638I is representative of the accused Samsung DDR SDRAM products; Samsung Part No. K4H510838C is representative of the accused Samsung DDR; SDRAM products; Samsung Part No. K4J52324QC is representative of the accused Samsung GDDR3 products; Samsung Part No. K4S56323LF is representative of the accused Samsung MOBILE SDR products; Samsung Part No. K4S281632F is representative of the accused Samsung SDR SDRAM products; Samsung Part No. K4X56163PF is representative of the accused Samsung MOBILE DDR products; Samsung Part No. M378T2953EZ3 is representative of the accused Samsung DDR2 modules products; Samsung Part No. K4T1G084A is representative of the accused Samsung DDR2 and gDDR2 products.

[5] Hynix Part No. HY5PS124(8,16)21FP is representative of the accused Hynix DDR2 SDRAM products and of all the accused Hynix GDDR3 SDRAM products, except for the GDDR3 product that is Part No. HY5RS573225F.

[6] Nanya Part No. NT5TU64M8AE is representative of the accused Nanya DDR2 SDRAM products.

[7] Micron Part Nos. MT47H16M16 and MT47H32M16 are representative of the accused Micron DDR2 products; Micron Part No. MT44H8M32 is representative of the accused Micron GDDR3 products; and Micron Part No. MT49H32M9 is representative of the accused Micron RLDRAM II products.

[8] There are differences between the Accused Products that are unrelated to the issues presented in this motion. By its Counterclaim in reply, Rambus has asserted that the Manufacturers' DDR3 and GDDR4 products infringe the Ware patents-in-suit. These counterclaims-in-reply are the subject of motions to strike made by Micron, Nanya and Samsung, who contend that DDR3 products should not properly be part of this case. The Manufacturers' respective motions to strike are set for hearing before the Court on October 26, 2007. Should the Court deny these motions, Manufacturers expect to seek leave to supplement their motions for summary judgment to include any newly added products.

Appendix A to the Manufacturers' claim construction brief, the transaction terms set forth in Appendix B to the Manufacturers' claim construction brief, or the clocking terms set forth in Appendix C to the Manufacturers' claim construction brief will render summary judgment of noninfringement appropriate.

A. Legal Framework for Summary Judgment of Noninfringement

Literal infringement requires that "every limitation recited in the claim appear[ ] in the accused product, *i.e.*, when the properly construed claim reads on the accused device exactly." *DeMarini Sports, Inc. v. Worth, Inc.*, 239 F.3d 1314, 1331 (Fed. Cir. 2001) (citation omitted). Infringement under the doctrine of equivalents requires there to be "insubstantial" differences between the accused products and the claim limitations or for the accused products to satisfy the "function, way, result" test. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.* 493 F.3d 1368, 1377 (Fed. Cir. July 5, 2007) (citing *Graver Tank & Manufacturing Co. v. Linde Air Products Co.*, 339 U.S. 605 (1950)).

Rambus bears the burden of proving infringement. *Exigent Tech., Inc. v. Atrana Solutions, Inc.*, 442 F.3d 1301, 1309-10 (Fed. Cir. 2006). As a result, the Manufacturers are not required to produce evidence showing the lack of a genuine issue of material fact. *Celotex Corp. v. Catrett*, 477 U.S. 317, 325 (1986). Rather, the Manufacturers only need to show "an absence of evidence to support the nonmoving party's case." *Id.* at 325. Rambus, as the nonmoving party, must "come forward with 'specific facts showing that there is a genuine issue for trial'" in order to successfully oppose this motion. *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986) (quoting Fed. R. Civ. P. 56(e)).

Summary judgment is "designed to secure the just, speedy and inexpensive determination of every action." *Celotex Corp. v. Catrett*, 477 U.S. 317, 327 (1986) (internal quotations omitted). The Manufacturers seek summary judgment of noninfringement based on each of the following three independent grounds: (1) there is no factual dispute that the Accused Products do not meet the "device" limitations, which should be construed to require an interface with a specific bus architecture (Section IV.B); (2) there is no factual dispute that the Accused Products do not meet the "transaction" limitations, which should be construed to require receipt of request

packets (Section IV.C); and (3) there is no factual dispute that the Accused Products do not meet the "clock" limitations, which should be construed to require use of an early clock / late clock scheme (Section IV.D).[9]

B. The Accused Products Do Not Comprise the "Device" Required by the Asserted Claims

The Manufacturers' proposed construction of the term "device," a fundamental term contained in each of the asserted claims,[10] is "electronic circuits or components with [1] a bus interface that is adapted to connect to a multiplexed set of signal lines, each for carrying address, data, and control information, [2] that has substantially fewer connections to signal lines than the number of bits in a single address, and [3] that does not connect to a separate device select line.[11]

If adopted, this construction will render summary judgment of noninfringement appropriate for the following three independent reasons: [1] the Accused Products are not triple-multiplexed to carry control, address and data over the same signal lines; separate sets of control, address, and data lines are used; [2] the Accused Products do not have substantially fewer signal lines than number of bits in a single address; rather the number of lines in the Accused Products that carry address, data, or control information is greater than or approximately equal to the number of bits in an address; and [3] the Accused Products have at least one dedicated device select line.

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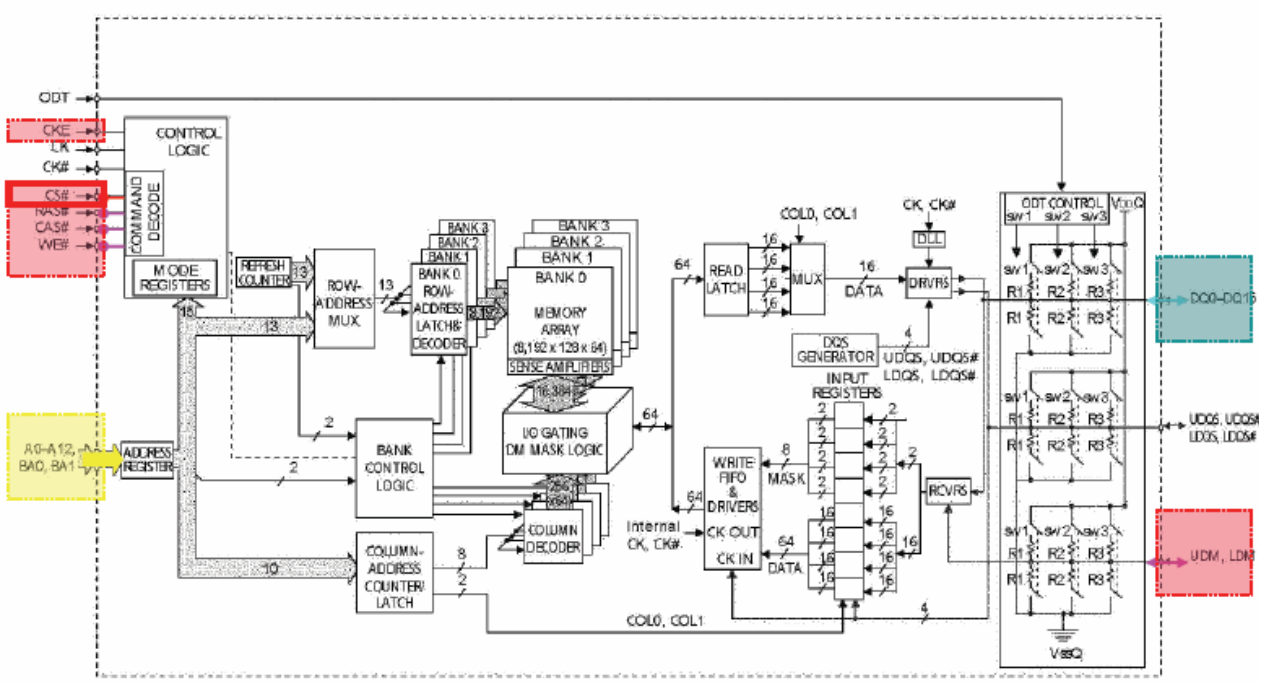
[9] While there are no factual disputes regarding the structure and operation of the Accused Products relevant to the issues presented in this motion, there may be factual disputes regarding the Accused Products with respect to other issues that may arise in this litigation, including factual issues with respect to these claim limitations if the Court adopts Rambus's proposed constructions.

[10] The term "device" is a part of several disputed terms of the Farmwald patent claims, such as "integrated circuit device," "memory device," "controller device," and variations thereof. *See* App. A to Manufacturers' Responsive Brief on Claim Construction ("Mfr. CC Br."), filed September 14, 2007.

[11] The Manufacturers have adopted a single consolidated construction to narrow the issues in dispute. By supporting the Manufacturers' construction of the "device" terms, Hynix does not waive, but maintains, both its objections to the Court's constructions of the analogous "device" terms in Case No. CV 00-20905 and its arguments that, absent such a construction of the "device" terms, all of Rambus's patent claims containing such terms are invalid under the written description requirement of 35 U.S.C. ¶ 112.

1. The Manufacturers' Accused Products Are Not Triple-Multiplexed To Carry Control, Address, and Data Over the Same Lines, as Required by the Proper Construction of the Term "Device"

Faithful to the disclosure of the purported invention in the Farmwald specification as well as its explicit characterization of "the invention," the Manufacturers' proposed construction of "device" requires that the electronic circuits or components include "a bus interface that is adapted to connect to a multiplexed set or signal lines, each for carrying address, data, and control information …." Mfr. CC Br. at 9-15. In other words, the proper construction of the term "device" requires a bus interface that connects to a set of signal lines that are each triple-multiplexed to carry address, data and control information over the same signal lines. The Accused Products do not satisfy this limitation.



See Declaration of John Beynon In Support Of The Manufacturers' Joint Motion For Summary Judgment of (1) Non-Infringement of The Farmwald Patents Under The Manufacturers' Proposed Claim Constructions, or (2) Invalidity Of the Farmwald Patents Under Rambus's Proposed Claim Construction ("Beynon Decl.") Exh. 1 [Micron Datasheet], p. 16.

Rather, as illustrated by the functional block diagram[12] reproduced above for a Micron DDR2 SDRAM by way of example, none of the signal lines in the Accused Products is triple-multiplexed (that is, no signal line carries address, control and data). In particular, under the normal and intended use of this memory: none of the data lines (shown in blue) carry address or control information; none of the control lines (shown in pink) carry address or data; and none of the address lines (shown in yellow) carry data.[13] McAlexander SJ Decl. ¶ 81-86. This is the conventional structure for a DRAM memory. *Id.*

This structure is fundamentally different from the narrow multiplexed bus claimed in the Farmwald patents-in-suit. As noted above, during normal operation, the Accused Products function in a substantially different way, using a wide set of separate, dedicated buses in which no single line is triply multiplexed. McAlexander SJ Decl. ¶ 86-87.

2. The Manufacturers' Accused Products Do Not Have Substantially Fewer Signal Lines than the Number of Address Bits

In accordance with the disclosure of the purported invention in the Farmwald specification, the Manufacturers' proposed construction of "device" also requires that the "bus interface . . . has substantially fewer connections to signal lines than the number of bits in a single address . . . ." Mfr. CC Br. at 9. The Accused Products do not meet this construction because they in fact have an equal or greater number of signal lines (*i.e.*, address, data and control signal lines) than the number of bits in a single address.

Memories are organized in arrays having rows and columns. A particular memory location – a "cell" in the array – is addressed by a row address and a column address. McAlexander SJ Decl. ¶ 90. Memories are also arranged in "banks," with each bank containing a memory array. Therefore, the bank addresses are also needed when addressing a memory cell so

[12] This is a diagram from the Micron MT47H32M16 DDR2 datasheet. This functional block diagram is intended to aid in understanding the connections, inputs, and outputs of the memory. It does not represent an actual circuit implementation. Not all Manufacturers' Accused Products have the same number of address signal lines, bank address signal lines, data signal lines, and data mask signal lines as illustrated in this figure.

[13] Data is that information that is written to or read from the memory array; it is always sent on the data lines. McAlexander SJ Decl. ¶ 81-82.

that the memory knows which bank the cell is in as well as the particular cell location within the array. *Id.* Given this addressing scheme, the number of bits in a single address is calculated by adding (1) the number of bits in the row address, (2) the number of bits in the column address, and (3) the number of bits in the bank address. *Id.*

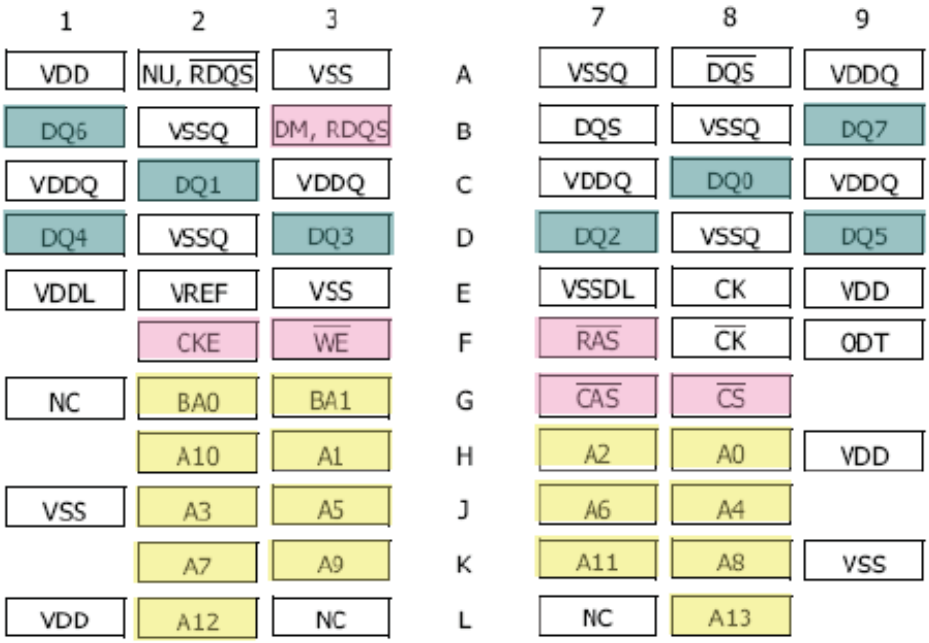
Reference to a datasheet for a Hynix memory is illustrative of this point:

ROW AND COLUMN ADDRESS TABLE

ITEMS	64Mx8
# of Bank	4
Bank Address	BA0, BA1
Auto Precharge Flag	A10/AP
Row Address	A0 - A13
Column Address	A0-A9
Page size	1 KB

Beynon Decl. Exh. 3 [Hynix Datasheet], p. 6.

In this example, adding the 14 bits of row addresses (A0-A13) to the 10 bits of column addresses (A0-A9) to the 2 bits of bank addresses (BA0-BA1) provides a total of 26 bits used to specify an address in this Hynix memory. The diagram below from the same datasheet represents the pins (connections) corresponding to each signal line. There are 6 control signal lines shown in pink (/CS, /CAS, /RAS, /WE, DM and CKE), 16 address signal lines shown in yellow (A0-A13 which are used to send row and column addresses and BA0-BA1 which are used to send bank addresses) and 8 data signal lines shown in blue (DQ0-7), for a total of 30 signal lines. Thus, this product has 30 signal lines, which is more than the 26 bits required to specify an address.



1	2	3		7	8	9
VDD	NU, $\overline{RDQS}$	VSS	A	VSSQ	$\overline{DQS}$	VDDQ
DQ6	VSSQ	DM, RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	$\overline{WE}$	F	$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1	G	$\overline{CAS}$	$\overline{CS}$	
	A10	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

Beynon Decl. Exh. 3 [Hynix Datasheet], p. 8.

As demonstrated in the accompanying McAlexander declaration, each of the Accused Products has at least the same number of signal lines as the number of bits necessary to specify an address, and most have more signal lines than the number of bits necessary to specify an address. An equal or greater number cannot be "substantially fewer." McAlexander SJ Decl. ¶ 93. Therefore, the Accused Products do not meet the "substantially fewer connections to signal lines" requirement of the Manufacturers' proposed construction of the term "device." *Id.* at 95.

Because the Accused Products do not have "substantially fewer connections to signal lines," as required by the claims, the differences between the asserted claims and Accused Products are not insubstantial. *Id.*

3. The Manufacturers' Accused Products Have at Least One Dedicated Device Select Line

Following the disclosure of the purported invention in the Farmwald specification, the Manufacturers' proposed construction of "device" also requires that the "bus interface . . . does not connect to a separate device select line." Mfr. CC Br. at 9.

The Accused Products cannot satisfy this limitation because, as illustrated in the foregoing pinout diagram of an accused Hynix memory by way of example, each of the Accused Products

has at lease one separate device select line, called "chip select" or "/CS" (shown within a red box in the illustration above). McAlexander SJ Decl. ¶ 97; see also Beynon Decl. Exh. 2 [Samsung Datasheet]. The "chip select" line is a dedicated line that indicates when the particular memory chip is to read the information sent by the controller. This line is used for no other purpose. McAlexander SJ Decl. ¶ 99 Each of the Accused Products has at least one connection to a chip select line. *Id*. ¶ 97. None of the Accused Products embed device identification information in the address or otherwise in the requests that identify the chip or set of chips out of all the chips in a memory system to which the request is directed. *Id*. ¶ 101.

The use of the "chip select" line in the Manufacturers' products differs substantially from the claimed inventions, which specifically claim a device in which such lines are not present. *Id*. ¶ 102.

C. The Accused Products Do Not Receive The Transaction Request Packets Required by the Asserted Claims

Summary judgment of noninfringement is also appropriate based on the Manufacturers' proposed constructions for the "transaction" terms (*e.g.*, read request and write request), because the Accused Products do not receive the request packets or transmit address and control information in a packet as required by the entirety of the Farmwald specification and each of the asserted claims.

Each of the asserted claims is directed to sending information to or from a memory device, and specifies the type of transaction to be performed (*e.g.*, a read or a write) and/or the type of information sent to the memory device as part of the transaction request (*e.g.*, address or control information). Under the Manufacturers' proposed constructions for the transaction request terms, each of the asserted claims requires the request and associated information to be sent in the form of a request packet. As explained in the Manufacturers' claim construction brief, the entirety of the common Farmwald specification describes the transaction requests and information included therein as sent to the memory devices in the form of request packets, and never describes the transaction requests in any other way, or even suggests any other format.

For example, claim 1 of the '285 patent is directed to a "method of operation in a memory device" comprising "receiving a request for a write operation."[14] The Manufacturers' proposed construction for "request for a write operation" requires that the information used to request the write operation be sent in the form of a request packet. Likewise, the Manufacturers' proposed constructions for all of the other transaction terms set forth in Appendix B to the Manufacturers' claim construction brief (*e.g.*, "read request" and "block size information") also require that the information used to specify the transaction to be performed (*e.g.*, a read operation) and the information sent therein (*e.g.*, the block size information required for that read operation) be sent in the form of a request packet.

1. A Request Packet is a Contiguous Series of Bytes And Must Follow a Predefined Packet Format

A packet is a contiguous series of bytes (*i.e.*, chunks of "1"s and "0"s) in which each bit of information (*i.e.*, each "1" and each "0") has a predefined meaning based on its position within the packet. *See* McAlexander SJ Decl. ¶ 104. This is consistent with the common Farmwald specification's definition of "request packet" as "a contiguous series of bytes containing address and control information." '184 patent at 8:61-62; *see also Rambus, Inc. v. Infineon Tech., Inc.*, 318 F.3d 1081, 1092 (Fed. Cir. 2003) ("the request packet, which the specification defines as 'a contiguous series of bytes containing address and control information'").

For each of the bits sent within a packet to have meaning to the device that receives the packet, the packet must include information (*e.g.*, a header) identifying the type of packet it is, and there must be a predefined format for that type of packet specifying the meaning of each bit of information within the packet based on its position within the packet. McAlexander SJ Decl. ¶ 104. The predefined format must specify the size of the packet so that the device knows when the packet starts and ends, and the meaning of each bit in the packet based on its position within the packet. *See id.* Without a predefined format, it would be impossible for the receiving device

[14] Other asserted claims, for example, are directed to receiving an "operation code," which the parties agree specifies the type of transaction to be performed (*i.e.*, a read or a write).

to determine the type of information within the packet, including when the packet starts and ends. *See id*. Otherwise the contiguous series of bytes would be a meaningless set of "1"s and "0"s.

Figure 4 of the Farmwald patents-in-suit illustrates a packet. *See* '184 patent at 9:24-65; Figure 4; *see also* McAlexander SJ Decl. ¶ 107. The start of the request packet is specified by setting the "AddrValid" field to "1" in an otherwise unused clock cycle. *Id.* The "AccessType" field in the packet defines the type of request, and the "Master" field identifies the master sending the request packet. *Id.* When the device to which the packet receives the request packet it decodes the packet according to the established protocol, and example of which is shown in Figure 4. For example, the format shown in Figure 4 specifies that the first bit of the AccessType field indicates whether the request is a read or a write, and that the bits sent during the second bus cycle specify the first nine bits of the address.

While the specific format described in the packet and illustrated in Figure 4 is only a preferred embodiment of a format for a request packet, each of the requests received by the claimed memory device must follow a predefined format in which the meaning of each bit in a contiguous series of bytes is derived from its position relative to the other information in the packet. McAlexander SJ Decl. ¶ 104. Without a predefined format for each type of packet, it would be impossible for the memory device to determine the meaning of transactions sent as a contiguous series of bytes. *Id.* ¶ 108.

2. The Accused Products Do Not Receive Request Packets

The commands and other information received by the Accused Products, in contrast, are not in the form of request packets. *See* McAlexander SJ Decl. ¶ 109. The Accused Products do not receive contiguous series of bytes which derive meaning from a predefined format. *Id.* Nor do the Accused Products decode information based on a packet protocol. *Id.* ¶ 107. Rather, the communications protocol that governs communications to the Accused Products is a dedicated bus system using point-to-point bus system based on signaling in which the signals sent to the Accused Products acquire meaning based on the combined state of a set of dedicated signal lines and the current state of the Accused Product.. *See id.* ¶ 108.

In contrast to packets, the commands received by the Accused Products do not include information defining the type of information being sent. Nor is there a predefined format specifying the meaning of each bit of information for a predetermined number of clock cycles. McAlexander SJ Decl. ¶109. Rather, the information received by the Accused Products acquires meaning based on the combined state of the signal lines (each of which is dedicated to transmitting a particular type of information) for the clock cycle during which that information is received. *Id.*

For example, the /WE control line (write enable) is dedicated to specifying whether a command is a read or write. Assuming the other signal lines and the Accused Product are in the right state for a read or a write operation, then a low /WE line specifies a write and a high /WE line specifies a read. *See, e.g.*, Beynon Decl Exh. 3 [Hynix Datasheet] at 8. Similarly, address line A0 always specifies part of a row address if the /RAS control line is low and always specifies part of a column address if the /CAS control line is low. *Id.*

In contrast, as explained above in connection with the Farmwald invention, each of the contiguous bits in a packet derives its meaning based on its position within the packet relative to the other information in the packet. *See* McAlexander SJ Decl. ¶ 104. This is very different from the commands and other information received by the Accused Products, which derive their meaning based only on the combined state of a set of dedicated signal lines and the state of the Accused Product during the clock cycle during which each command is transmitted.

Because the Accused Products receive information in a substantially different format than as claimed in the Farmwald patents-in-suit, the dedicated bus protocol of the Accused Products is not equivalent to the packet-based protocol required by the patents.

D. The Accused Products Do Not Use The Early Clock / Late Clock Scheme Required by the Asserted Claims

The Manufacturers' proposed constructions for the "clocking" terms will also render summary judgment of noninfringement appropriate for all of the asserted claims. The term "external clock signal/external clock" appears in all the asserted claims of the Farmwald patents-in-suit, except '5,020 patent claims 1 and 2. The term "internal clock signal" appears explicitly in

four asserted claims ('051 patent claim 32; '037 patent claim 9; '295 patent claim 45; and '8,020 patent claim 36), and also appears in the Manufacturers' proposed constructions of other claim terms.[15] Only one asserted claim ('184 patent claim 14) includes neither "internal clock signal" nor a term the Manufacturers have construed to include "internal clock signal."

1. The Properly Construed Clocking Terms Require Two Different Clock Signals, an Early Clock and a Late Clock, from which Timing Information Can Be Derived

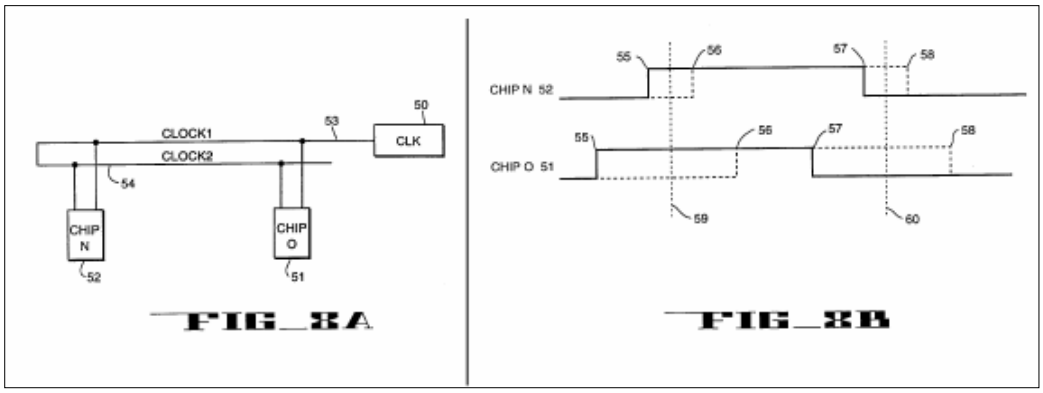
The Manufacturers' construction of the term "external clock signal/external clock" properly reflects the only clocking scheme disclosed in the Farmwald specification. In *Hynix I* this Court referred to Farmwald's sole clocking scheme as the "'early clock/late clock' system, which determines the distinct mid-point between the early and late clocks to establish a system clock signal that is temporally consistent regardless of device placement along the bus." *See* Mfr. CC Br. at 23 (quoting Court's *Hynix I* summary judgment order); McAlexander SJ Decl. ¶ 112. The Court held that this "early clock/late clock" system is "the only embodiment of the clock in the entire specification." *See* Mfr. CC Br. at 25 n.26 (quoting *Hynix I* CC Order). In accordance with the specification's description of Rambus's claimed invention, the Manufacturers' proposed construction of the term "external clock signal/external clock" is "a continuously periodic signal, from a source external to the device that provides an early clock and a late clock from which timing information can be derived."

The required early clock signal and late clock signal are two different clock signals, each with different timing information. Both of these different clock signals are necessary to provide the timing information on which the Farmwald clocking scheme depends to create the internal clock signal required by the claims. In *Hynix I* the Court provided a concise description of these two different clocks and how they are used to create the internal clock. *See* Mfr. CC Br. at 25 (quoting Clock SJ Order at 2:18-18).

[15] These terms include the following terms that were discussed in the Manufacturers' Responsive Claim Construction Brief: "output driver(s) circuitry," "input receiver(s) circuitry," "sample/samples/sampling," "clock alignment circuit," and "delay lock(ed) loop." *See* Mfr. CC Br. at 24.

The Court's description, and Figures 8A and 8B from the Farmwald specification to which the Court's description refers, are set forth below:

> Rather than connecting all devices on the bus to a single clock signal, Rambus discloses a U-shaped clock line which is connected to each device twice. The device's first clock connection receives its clock signal as the pulse travels out ("early clock"); the device's second clock connection receives its clocking information as the pulse travels back ("late clock"). *See, e.g.*, '152 patent, Fig. 8A. Each device on the bus samples the early and late clocks, and via internal circuitry, each device independently generates its own internal device clock by determining the midpoint between the external clocks; regardless of the inherent propagation delays in the bus design, every independently derived midpoint provides actual synchronous event timing for all devices on the bus. *See* '152 patent, fig. 8B, fig. 12, col. 19, ll. 6-9. Despite the fact that each device receives external clock signals exhibiting varying amounts of flight time induced clock skew, the independently derived midpoints, which act as the internal clocks within each device, establish a "true system clock" against which all bus devices operate.[16]



As the Court's explanation demonstrates, the timing information that is derived from the two different early and late clock signals is the internal clock signal. The Manufacturers' construction of the term "internal clock signal" properly reflects this relationship: "an internally created clock signal that is aligned with the midpoint of the early clock and late clock from the external clock signal."

[16] The Farmwald specifications describe the "U-shaped" bus clock line shown in Fig. 8A as a preferred embodiment of the early clock/late clock system, and describes an alternative embodiment of "[a] single bus clock line" which "is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal." '184 patent at 19:10-13. Both embody the same "early clock/late clock" system in which "[e]ach device must sample the two bus clocks and generate its own internal device clock at the midpoint of the two." *Id.* at 19:30-32; McAlexander Declaration In Support of the Manufacturers' Responsive Brief on Claim Construction, filed Sept. 14, 2007, ¶¶ 88-89.

2. The Accused Products Use a Fundamentally Different Clocking Scheme that Lacks the Required External Clock Signal and Internal Clock Signal

The clocking scheme used by the Accused Products is fundamentally different from Farmwald's "early clock/late clock" scheme. Unlike the Farmwald clocking scheme, the Accused Products do not receive an "early" and "late" clock nor do the Products derive timing information from "early" and "late" clock signals. Rather, the Accused Products use a single differential clock consisting of a clock signal and its inverted replica (*i.e.*, a "complement" of the clock signal which is 180 degrees out of phase from the actual signal).[17] McAlexander SJ Decl. ¶ 113. By using the clock signal and its "complement" (often referred to as a "differential clock"), a single point of timing information (at the crossing point of the rising and falling edge) is derived for receipt of addresses and commands as well as the approximate timing of data output from a single memory chip. *Id.* ¶ 115.

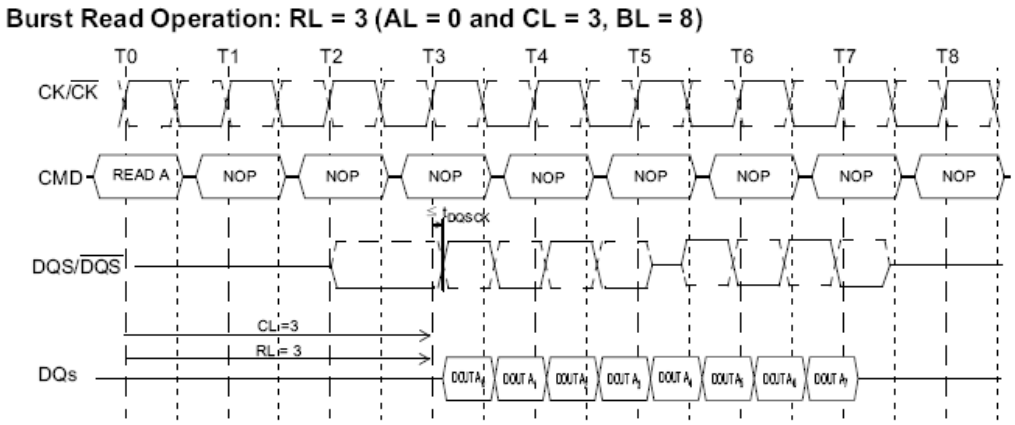
The following excerpt from a representative Hynix data sheet describes the clock signal (referred to as CK) and its complement which is the inverse of the same clock signal (referred to as $\overline{CK}$) as "differential clock inputs:

PIN	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).

McAlexander SJ Decl. ¶ 114; Beynon Decl. Exh. 3 [Hynix Datasheet], p. 8. Together CK and /CK represent a single timing signal.

This timing scheme is illustrated by the following drawing from a Hynix Device Operation & Timing Diagram for a Burst Read Operation:

[17] The Samsung single data rate products use a single external clock without using "differential" or "complementary" inputs. McAlexander SJ Decl. ¶ 114. In other words, the Samsung single data rate products only receive clock signal CK. The rising edge of the single external clock CK is the single point of timing information in these products. *Id.* Because these products do not receive an early and late clock, under the Manufacturers' constructions, these products do not meet the limitations of the "external clock/external clock signal" and "internal clock signal" claim terms.



McAlexander SJ Decl. ¶ 114; Beynon Decl. Exh. 4 [Hynix Device Operation & Timing Diagram for a Burst Read Operation], p. 22.

As shown, the timing references (T0-T8) are defined by the point where the falling edge of the clock, CK (dotted line), crosses the rising edge of complement $\overline{CK}$ (solid line). McAlexander SJ Decl. ¶ 114. CK and $\overline{CK}$ are not an "early" clock and "late" clock, i.e., different timing signals that arrive at different times and from which timing information is derived. *Id*. Rather, they are complements of the same clock signal representing a single timing reference. *Id*. Therefore, they do not comprise the required "external clock signal/external clock" of the asserted Farmwald claims.[18] *Id.* at ¶ 123. As a result, summary judgment of literal noninfringement is appropriate on all asserted claims that include the "external clock" terms (*i.e.*, all asserted claims except '5,020 patent claims 1 and 2). *DeMarini*, 239 F.3d at 1331.

In addition, because the required "internal clock signal" is derived from the "external clock signal," summary judgment of literal noninfringement is appropriate on all asserted claims

[18] The use of differential clock inputs simply makes the timing references more precise and less susceptible to noise and drift, thereby permitting higher operating speed. McAlexander SJ Decl. ¶ 113. Unlike the Farmwald "early clock/late clock" scheme,in which skew is eliminated between devices, such as memory devices (i.e., the timing is the same for each of the devices connected to the bus), the Manufacturers' Accused Products' single externally provided clock signal or differential clock signal do not eliminate skew between memories. *Id.* ¶ 121; *see* Mfr. CC Br. at 25 n.26 (Farmwald's clocking scheme was created specifically to minimize clock skew between multiple memory devices caused by their differing relative locations on the bus) (citing *Hynix I* CC Order at 29:25-30:1, 30:7-10). Rather than rely on a specialized clocking scheme to minimize skew between different memories in the system, the Accused Products rely, for example, on matching the lengths of clock and data signal lines to minimize skew. *Id.*

in which the term "internal clock signal" appears explicitly or as part of the Manufacturers' other proposed constructions incorporating the construction of "internal clock signal" (*i.e.*, all asserted claims except '184 patent claim 14). *Id.*

The use of the cross point of a complementary clock signal in the Accused Products does not eliminate clock skew between different memory chips in the system. Accordingly, it differs substantially from the use of an early clock and a late clock to align the memory in a system, as required by the Farmwald patents. *See* McAlexander Decl. ¶ 122. Summary judgment is, therefore, also appropriate on all the asserted claims under the doctrine of equivalents. *Festo*, 493 F.3d at 1377.

V. SUMMARY JUDGMENT OF INVALIDITY

As demonstrated herein and in the accompanying declaration of Joseph McAlexander, adoption of Rambus's proposed claim constructions for the "device" terms set forth in Appendix A to the Manufacturers' claim construction brief, the transaction terms set forth in Appendix B to the Manufacturers' claim construction brief, or the clocking terms set forth in Appendix C to the Manufacturers' claim construction brief will render summary judgment of invalidity appropriate under 35 U.S.C. § 112.

A. The Claims Are Invalid for Lack of Written Description Under § 112, ¶ 1

1. Legal Framework

Compliance with the statutory written description requirement, set forth in 35 U.S.C. § 112, ¶ 1, is essential for the validity of a patent. The purpose of the written description requirement is to "ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification." *Univ. of Rochester v. G.D. Searle & Co., Inc.*, 358 F.3d 916, 920 (Fed. Cir. 2004) *citing Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1345 (Fed. Cir. 2000)).

The written description requirement is premised on the fundamental notion that patents must provide notice to the public, in the initial application, consistent with the scope of the claims. To fulfill the written description requirement, the patent specification "must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of

the claimed invention at the time of the application, i.e., that the patentee invented what is claimed." *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). An applicant complies with the written description requirement by "such descriptive means as words, structures, figures, diagrams, formulas, etc., that fully set forth the claimed invention." *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) A narrow disclosure will limit claim breadth, because the scope of a claim cannot be "greater than what a person of skill in the art would understand the inventor to possess." *LizardTech*, 424 F.3d at 1346. The mandates of public notice do not allow any gaps between claim scope and the patent's disclosure to be satisfied by what those skilled in the art may consider to be "an obvious variant of that which is disclosed in the specification." *Lockwood*, 107 F.3d at 1572. "It is not sufficient for the purposes of the written description requirement of §112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to modifications that the inventor might have envisioned, but failed to disclose." *Id.*

Because the written description must provide notice of the boundaries of the claims, a patent's disclosure of a species does not necessarily provide sufficient written description support for a claim more broadly directed to the genus. The Federal Circuit emphasized this point in *Bilstad v. Wakalopulos*, 386 F.3d 1116, 1124-25 (Fed. Cir. 2004), where it provided two examples of disclosure of a species that would not support a genus claim. Although the court gave as one example "unpredictability in the particular field" (*id.* at 1125), *Bilstad* did not establish that "unpredictability in the art" is necessary for a finding of lack of enablement. Rather, *Bilstad* provided a second example where disclosure of a species would not support a genus claim: where the specification distinguishes the prior art as inferior and touts the advantage of a certain species. *Id.* In so doing, the court relied on *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998):

> Another exception [to disclosure of a species supporting a genus claim] is presented in *Tronzo* …. In *Tronzo*, this court held that substantial evidence did not support the jury's verdict that claims to a hip prosthesis of generic shape were supported by a parent disclosing only a trapezoidal shape. We said, "Instead of suggesting that the 589 patent [the parent] encompasses additional shapes, the specification specifically distinguishes the prior art as inferior and touts the advantages of the conical shape of the 589 cup. Such statements make clear that the 589 patent discloses *only* conical shaped cups and nothing broader."

Id.

The Federal Circuit has not hesitated to uphold summary adjudications of invalidity of patents that fail to adhere to the written description requirement. *See, e.g.*, *LizardTech*, 424 F.3d at 1346-47 (affirming grant of summary judgment of invalidity where patent specification's description of a particular method for creating a seamless discrete wavelet transform ("DWT") for digital image compression was insufficient as a matter of law to support disputed claim that broadly covered other methods of seamless DWT). In affirming the grant of summary judgment in *LizardTech*, the Federal Circuit also built upon the analysis of its earlier holding in *Tronzo*, which recognized that claims in a later-filed application are not entitled to the filing date of an earlier application under 35 U.S.C. § 120, unless the earlier application complies with the written description requirement. The *Tronzo* court held that, to meet the written description requirement, "the disclosure of the earlier application, the parent, must reasonably convey to one of skill in the art that the inventor possessed the later-claimed subject matter at the time the parent application was filed." *Id*. (emphasis added). *LizardTech* confirms that, although cases such as *Tronzo* dealt specifically with the issue of whether a patent was entitled to claim priority to a prior application, the test for satisfaction of the written description requirement is identical where, as here, the issue is whether claims issued in continuation applications are described in the parent specification. *See also Rochester*, 358 F.3d at 924 ("[T]he basic requirement of a written description of an invention exists whether a question of priority has arisen or not. The statute does not limit the requirement to cases in which a priority question arises.").

Thus, although compliance with the written description requirement is a question of fact, summary judgment is appropriate in cases such as this, where it is beyond dispute that the narrow description in the patent specification cannot support claims of broader scope. *See LizardTech*,

424 F.3d at 1346; *Rochester*, 358 F.3d at 927 (noting that "a patent can be held invalid for failure to comply with the written description requirement, based solely on the language of the patent specification"). "After all, it is in the patent specification where the written description requirement must be met." *Rochester*, 358 F.3d at 927.

2. Rambus's Proposed Constructions for the "Device" Terms Are Not Supported by the Specification Under § 112, ¶1

Rambus's proposed constructions for the "device" terms[19] would result in claims that bear little correlation to the specification. In particular, the Farmwald specification has no support for a broad device that interfaces with anything other than a narrow multiplexed bus. Throughout the specifications of the Farmwald patents-in-suit the purported invention is described as based on or including a specific, high-speed multiplexed bus architecture (referred to herein as the "narrow, multiplexed bus," which is shorthand for the characteristics of the bus architecture of the invention reflected in the Manufacturers' proposed construction of "device"), or devices interfacing to such a bus. The only discussion or mention in the Farmwald specifications of any other type of bus or bus interface occurs in the section of the specifications entitled "Comparison With Prior Art" ('184 patent at 2:6-3:21); in each case, the type of prior art bus mentioned is distinguished from the bus and bus interface that is later described in the specifications as the "present invention." McAlexander SJ Decl. ¶ 127.

Throughout the "Summary of the Invention" ('184 patent at 3:50-4:56), the "Detailed Description" (*id.* at 5:26-24:25), and the section of the specification reciting the "objects of the invention" (*id.* at 3:22-48), the "invention" is described as based on or including the narrow, multiplexed bus, or devices interfacing to such a bus. For example, the Summary of the Invention makes this clear from the beginning:

[19] Rambus does not propose a construction for the term "device" itself, insisting that no construction is warranted, and instead proposes construction for phrases incorporating device, such as "integrated circuit device," and "memory device."

> The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

Id. at 3:51-61 (emphasis added). This construction additionally follows from the objects of the invention:

> One object of the present invention is to use a new bus interface built into semiconductor devices to support high-speed access to large blocks of data from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner.
>
> Another object of this invention is to provide devices, especially DRAMs, suitable for use with the bus architecture of the invention.

Id. at 3:22-26, 3:46-48 (emphasis added). The Summary of the Invention continues:

> In the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus. Each memory device contains only a single bus interface with no other signal pins. Other devices that may be included in the system can connect to the bus and other non-bus lines, such as input/output lines. The bus supports large data block transfers and split transactions to allow a user to achieve high bus utilization. This ability to rapidly read or write a large block of data to one single device at a time is an important advantage of this invention.

Id. at 4:10-20 (emphasis added).

> The DRAMs that connect to this bus differ from conventional DRAMs in a number of ways. Registers are provided which may store control information, device identification, device-type and other information appropriate for the chip such as the address range for each independent-portion of the device. New bus interface circuits must be added and the internals of prior art DRAM devices need to be modified so they can provide and accept data to and from the bus at the peak data rate of the bus. This requires changes to the column access circuitry in the DRAM, with only a minimal increase in die size.

Id. at 4:21-31 (emphasis added). The Detailed Description likewise provides a consistently narrow description of the "present invention":

> The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system. The invention can also be used to connect processing devices and other devices, such as I/O interfaces or disk controllers, with or without memory devices on the bus. The bus consists of a relatively small number of lines connected in parallel to each device on the bus. The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using

> the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024 bytes) can be sent over a small number of bus lines (8 plus one control line in the preferred implementation).

Id. at 5:29-50 (emphasis added). *See also* McAlexander SJ Decl. ¶ 127-28.

In short, circuits or components with an interface to the narrow, multiplexed bus described in the Farmwald specifications are the only memory system embodiment disclosed. The original application says as much: "Many of these details have been implemented selectively in certain fast memory devices, but never in conjunction with the bus architecture of this invention." '184 patent at 23:62-65 (emphasis added); McAlexander SJ Decl. ¶ 131. There is no evidence that the specification contemplates devices that interface with a generic bus. Accordingly, a person skilled in the art would not understand Rambus to have invented such devices. McAlexander SJ Decl. ¶ 136-37.

If Rambus's broad construction of the "device" terms were accepted, the claims would cover a broad range of devices that interface with a generic bus – which is not and cannot be supported by the 1990 Farmwald specification. In that regard, the inadequacy of the specification to support Rambus's proposed construction in this case is similar to the failure of support identified in *LizardTech*, 424 F.3d 1336. In that case, the patent-at-issue pertained to wavelet transforms used in compression of digital images. *Id*. at 1337. The specification described a particular process for creating a wavelet transform; but the disputed claim more broadly recited a generic technique. *Id*. at 1345. In affirming the district court's grant of summary judgment of invalidity of that claim, the Federal Circuit explained that allowing the broad claim to stand in the absence of supporting disclosure would violate the Supreme Court's directive that the patentee "should understand, and correctly describe, just what he has invented, and for what he claims a patent.'" *Id*. at 1346 (quoting *Merrill v. Yeomans*, 94 U.S. 568, 573074 (1876)). Similarly, here, what Rambus purported to invent – and told the industry and investors that it invented years before litigation – were devices that interface with a narrow, multiplexed bus. *See* Mfr. CC Br. at

14-15. The written description bears this out. The Farmwald patents-in-suit, however, were filed a decade (or more) after the filing of the original Farmwald application as part of Rambus's flurry of industry-targeted patent filings, which presented a whole new range of claims that veered sharply away from the original disclosure. Rambus's after-the-fact, litigation-driven attempt to craft broader claims to cover non-Rambus memory technologies has resulted in claims that fatally deviate from the written description and must be invalidated. Summary judgment is appropriate.

Rambus also attempts with its broad proposed constructions of the "device" terms to read its claims onto devices that have a separate device select line. There is also no support in the specification for this broad construction. To the contrary, the original Farmwald specification consistently describes a system in which there is no separate device select line where all interface signals are bused. *See, e.g.*, '184 Patent at 3:51-61.

3. Rambus's Proposed Constructions for the Transaction Terms Are Not Supported by the Specification Under § 112, ¶1

If the Court adopts Rambus's proposed constructions for the transaction terms set forth in Appendix B to the Manufacturers' claim construction brief, each of the asserted claims is invalid under § 112, ¶ 1 for lack of an adequate written description because the Farmwald specification does not support sending transaction requests in any form other than request packets. *See LizardTech*, 424 F.3d at 1346 (scope of a claim cannot be "greater than what a person of skill in the art would understand the inventor to possess").

Throughout the Farmwald specification, the transaction requests sent to the memory devices are consistently and repeatedly described as part of request packets, and are never described in any other way. *See, e.g.*, '184 patent at 8:59-62; 8:66-9:4; 9:11-13; 12:45-48; 12:51-55; 13:4-6; 16:34-38; 16:62-65; 20:17-21; 20:32-38; 20:46-49; 21:28-31; 22:21-23. There is no disclosure anywhere in the specification of how to send information to a memory device other than within a request packet. *See* McAlexander SJ Decl. ¶ 104. As a result, one of ordinary skill in the art would not have understood Rambus to have invented a device capable of receiving transaction requests in any form other than a packet, which is a contiguous series of bytes interpreted according to a predefined format. *Id.* ¶ 104.

4. Rambus's Proposed Constructions for the Clocking Terms Are Not Supported by the Specification Under § 112, ¶ 1

The Farmwald specification discloses only one clocking scheme, which this Court referred to in *Hynix I* as "Rambus's 'early clock/late clock' system, which determines the distinct mid-point between the early and late clocks to establish a system clock that is temporally consistent regardless of device placement along the bus." *See* Mfr. CC Br. at 23 (quoting Court's *Hynix I* summary judgment order); McAlexander SJ Decl. ¶ 144. In fact, the specification expressly distinguishes "[t]he clocking scheme used in this invention" from previously known clocking schemes and asserts that the early clock/late clock scheme "has not been used before and in fact would be difficult to implement in backplane buses due to the signal degradation caused by connector stubs." *Id ¶ 145.*

When construing the Farmwald claims in *Hynix I*, this Court held that "the only embodiment of the clock in the entire specification required two external signals containing different information in order to create an internal clock, thus correcting the clock skew problem." *Hynix I* CC Order at 30:7-10 (quoting *Rambus, Inc. v. Infineon Techs. AG*, 2001 WL at 34138091 at *26 (E.D. Va. 2001) ("*Infineon I*"). Dr. Horowitz, one of the inventors, testified[20]

> Q Well, the early clock/late clock arrangement is the only external clocking scheme that's disclosed in the patent; right?
>
> A To the best of my recollection, that's correct.
>
> Q. And basically this Figure 12, you might have two of these Figure 12s in a particular device to generate two internal clocks?
>
> A. That's correct.
>
> Q But this is basically the only way—the only thing that's disclosed in the patent for generating those internal clocks that operate the input samplers and the output drivers?
>
> THE WITNESS: That's correct. To the best of my recollection, that figure [12] and the text relating to that figure is the part of the patent specification that describes how you generate clocks.

[20] Inventor testimony can be probative as to whether a patent specification satisfies the written description requirement of § 112, ¶ 1. *See New Railhead Mfg, LLC v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1295 (Fed. Cir. 2002) (approving of the district court's use of admissions made in the inventor's deposition testimony in finding lack of written description).

Beynon Decl. Exh. 5 [Transcript of Horowitz Deposition on April 30, 2004] at 105:12-106:5 (objections omitted); *see also id.* at 89:2-91:21. The single-minded focus on this one clocking scheme continues throughout the specification.

a. The Early Clock / Late Clock System Is the Only Solution Disclosed in The Farmwald Specification for Controlling Clock Skew

The specification discloses only the "early clock/late clock" system because the inventors viewed it as a critical component necessary to their invention. The specification explains that this specific clocking scheme is required to implement the high-speed multiplexed bus of the invention. *See, e.g.*, '184 patent at 3:28-30 (an "object of this invention is to provide a clocking scheme to permit high-speed clock signals to be sent along the bus with minimal clock skew between devices") (emphasis added). The specification explains that the purpose of this new clocking scheme was to avoid the "propagation delays" inherent in the single clock systems of the prior art:

> Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks. . . .
>
> [E]ach device must sample the two bus clocks and generate its own internal device clock at the midpoint of the two.

Id. at 18:62-19:3; 19:30-32 (emphasis added). The inventors needed a clocking scheme that would avoid propagation delays because a fundamental aspect of their invention was controlling "clock skew" between devices on the high-speed multiplexed bus. Again, the specification explains the specific clocking scheme's role in implementing this aspect of the invention:

> One important part of the input/output circuitry generates an internal device clock based on early and late bus clocks. Controlling clock skew (the difference in clock timing between devices) is important in a system running with 2 ns cycles, thus the internal device clock is generated so the input sampler and the output driver operate as close in time as possible to midway between the two bus clocks.

Id. at 22:50-56 (emphasis added). Dr. Farmwald testified accordingly:

> The invention, both my recollection of it and just reading it, describes what it views as an improvement on the standard way of clock (sic), which doesn't take into account the systematic skew, which is this generation of the midpoint by using two clock signals.

Beynon Decl. Exh. 6 [Transcript of Farmwald Deposition on January 22, 2004] at 39:21-40:1; *see also id.* at 37:11-38:18 (explaining "systematic skew" inherent in clock lines, identifying that skew as "a noticeable amount of delay" in a high-speed system, and explaining how the "early clock/late clock" system solves the problem).

As noted above, this Court found in *Hynix I* that the specific "early clock/late clock" system was created to correct the clock skew problem. *Hynix I* CC Order at 30:7-10. The Court also explained why eliminating clock skew was necessary to implement the claimed inventions:

> To operate the Rambus bus architecture at high speed, "[e]very system, every … chip, every component on the bus has to be operating under the exact same timing constraints. That's why it's important and valuable … to use a clock design that will synchronize everything together."

Id. at 29:25-30:1 (quoting *Infineon I*, 2001 WL at 34138091 at *26 n.38 (E.D. Va. 2001)). The specification's disclosure of the "early clock/late clock" system, and only that system, was no mistake or oversight. It was the inventors' deliberate attempt to direct those skilled in the art to the only clocking scheme that they thought would meet the objectives of their invention. *See, e.g.,* '184 patent at 3:8-11 ("The clocking scheme used in this invention has not been used before. . . .) (emphasis added)

b. One Skilled in the Art Would Not Recognize the Purported Invention As Including a Clocking Scheme Other Than the Early Clock / Late Clock Scheme

If the Court were to adopt Rambus's broad constructions of "clocking" terms, the claims would cover clocking schemes well beyond the "early clock/late clock" system disclosed in the specification.[21] Indeed, Rambus's constructions would cover the very prior art clocking schemes with the "clock skew" problem that the inventors intended their specific early clock/late clock system to overcome. McAlexander SJ Decl. ¶ 153. If so construed, the claims that include clocking terms would be invalid as a matter of law for failing to meet the written description

[21] For example, Rambus's proposed construction of "external clock signal/external clock" is "a periodic signal from a source external to the device to provide timing information." JCCS, App. A, Term No. 17. Rambus's proposed construction of "internal clock signal" is "a periodic or gated periodic signal generated in a device to provide timing information for internal operation." *Id.*, Term No. 23.

requirement of 35 U.S.C. § 112, ¶ 1. The specification does not "reasonably convey to one of skill in the art" that the inventors considered other clocking schemes to be within the scope of their invention at the time they filed the '898 Application (April 18, 1990). *Tronzo*, 156 at 1158; McAlexander SJ Decl. ¶ 155. Rather, as demonstrated above, the specification teaches one of ordinary skill the contrary; *i.e.*, that the purported newly disclosed early clock/late clock clocking scheme, not the prior art clocking schemes, was the only scheme that the inventors disclosed that solves the clock skew problem to achieve the objectives of the invention

This issue is governed by *Tronzo*, where the subject patent specification disclosed only a conically-shaped cup in a hip prosthesis. 156 F.3d at 1158-59. The only reference in the specification to different shapes was a recitation of the prior art. *Id.* at 1159. The Federal Circuit held that:

> Instead of suggesting that the 589 patent [the parent] encompasses additional shapes, the specification specifically distinguishes the prior art as inferior and touts the advantages of the conical shape of the 589 cup.

Id. The Federal Circuit gave the following example of how Tronzo's specification distinguished prior art and touted the conical shape:

> Another extremely important aspect of the present device resides in the configuration of the acetabular cup as a trapezoid or a portion of a truncated cone.

Id. (quoting Tronzo's specification). The Federal Circuit held that:

> Such statements make clear that the 589 patent discloses *only* conical shaped cups and nothing broader. The disclosure in the '589 specification, therefore, does not support the later-claimed, generic subject matter in claims 1 and 9 of the '262 patent.

Id.

The Farmwald specifications' statements concerning the early clock/late clock system are remarkably similar to Tronzo's statement on which the Federal Circuit based its holding of lack of written description. The specification makes clear that "[t]he DRAMs that connect to this bus differ from conventional DRAMs in a number of ways," including the use of the early clock/late clock circuit "to generate a low skew internal device clock for devices on the bus." '184 patent at

4:21-22, 31-32 (emphasis added). The specification emphasizes the importance of the early clock/late clock scheme to the invention:

> [An] object of this invention is to provide a clocking scheme to permit high-speed clock signals to be sent along the bus with minimal clock skew between devices.

id. at 3:28-30 (emphasis added).

> [An] important part of the input/output circuitry generates an internal device clock based on early and late bus clocks" to control "clock skew," which is "important in a system running with 2 ns cycles, thus the internal device clock is generated so the input sampler and the output driver operate as close in time as possible to midway between the two bus clocks.

id. at 22:50-56 (emphasis added).

Statements such as these teach one of ordinary skill that clocking schemes that lack early and late clocks, and that do not internally create a signal aligned with the "midpoint" of the early clock and late clock, will not achieve the objects of the invention. McAlexander SJ Decl. ¶¶ 144, 155. Rambus cannot, therefore, rely on the knowledge of one skilled in the art to argue that other clocking schemes are "inherently" disclosed in the specification. Again, *Tronzo* is on point:

> In order for a disclosure to be inherent . . . the missing descriptive matter must necessarily be present in the parent application's specification such that one skilled in the art would recognize such a disclosure. There is nothing in the '589 specification to suggest that shapes other than conical are necessarily a part of the disclosure. Indeed, as discussed above, the specification clearly suggests the contrary by asserting advantages of the conical shape over prior art shapes.

Tronzo, 156 F.3d at 1159.

In *LizardTech*, the Federal Circuit held that:

> The trouble with allowing claim 21 to cover all ways of performing DWT-based compression processes that lead to a seamless DWT is that there is no support for such a broad claim in the specification. The specification provides only a single way of creating a seamless DWT, which is by maintaining updated sums of DWT coefficients. There is no evidence that the specification contemplates a more generic way of creating a seamless array of DWT coefficients.

424 F.3d at 1344 (emphasis added). The same is true here: there is no evidence that the Farmwald specification contemplates a more generic clocking scheme than the "early clock/late clock" system; the only evidence is to the contrary. Rambus's broad constructions of the

clocking terms, if adopted, render all claims that contain them invalid as a matter of law under 35 U.S.C. § 112, ¶ 1.

B. The Claims Are Invalid for Failure to Claim the Subject Matter Which the Inventors Regarded as Their Invention Under § 112, ¶ 2

If the claims are construed as Rambus requests, they are invalid under 35 U.S.C. § 112, ¶ 2, which provides that: "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2 (emphasis added). The Federal Circuit has held that "[w]here it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention, [the court] must hold that claim invalid under § 112, paragraph 2." *Allen En'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002). While this requirement is related to the written description requirement of § 112, ¶ 1, the determination under §112, ¶ 2, "like a determination whether a claim is sufficiently definite, 'is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims.' Thus, as with claim construction, a determination under either portion of Section 112, second paragraph, is a question of law . . .." *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1377 (Fed. Cir. 2000) (quoting *Personalized Media Communications, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 705 (Fed. Cir. 1998) (citations omitted)).

The above analysis of the Farmwald specification proves that the subject matter which the applicants regarded as their invention was limited to (1) a device that interfaces only with a narrow, multiplexed bus; (2) a packet-based system that does not enable transfer of information other than in request packets; and (3) a clocking scheme limited to an "early clock/late clock" aimed at solving the "clock skew" problem of other clocking schemes. The specification shows that the inventors did not consider generic buses, information transfer protocols, or clocking schemes to be within the subject matter of what they purportedly invented. Rambus's proposed constructions would, however, encompass such subject matter and would render the claims invalid under §112, ¶ 2. *Allen Eng'g.*, 299 F.3d at 1349.

Regardless of how the Court decides the written description defense under § 112, ¶ 1, the Court must decide the defense under § 112, ¶ 2 as a matter of law. *Solomon*, 216 F.3d at 1377. If the Court adopts Rambus's constructions, the Court should grant the Manufacturers summary judgment of invalidity on this defense.

VI. CONCLUSION

For the foregoing reasons, the Manufacturers request that the Court grant summary judgment that the Manufacturers' Accused Products do not infringe the asserted claims if those claims are properly construed as proposed by the Manufacturers. In the alternative, should this Court adopt Rambus's proposed constructions for the "device," "transaction," or "clocking" disputed terms, the Manufacturers request that the Court grant summary judgment of invalidity based on the failure of the asserted claims to satisfy the written description requirement of 35 U.S.C. § 112, ¶ 1 and /or § 112, ¶ 2.

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